UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,523	07/03/2003	Simeon Furrer	CH920000067US1	7648

48813   7590   05/14/2009
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EXAMINER
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ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
05/14/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

pair@tuchmanlaw.com

	Application No.	Applicant(s)
Office Action Summary	10/614,523	FURRER ET AL.
	Examiner	**Art Unit**	
	LAWRENCE B. WILLIAMS	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>02 December 2008</u>.
2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>1-22 and 28</u> is/are pending in the application.
    4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) <u>1-22, 28</u> is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a) ☐ All   b) ☐ Some * c) ☐ None of:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____.
      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____ .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on
> sale in this country, more than one year prior to the date of application for patent in the United States.

2.   Claims 1-9, 16-22, 28 are rejected under 35 U.S.C. 102(b) as being anticipated by

Meinecke et al. (US Patent 5,319,754).

(1) Regarding claim 1, Meinecke et al. discloses communication device for processing

outgoing and incoming packets, the device comprising: a plurality of signal processing (HSRT)

units connected in sequence (col. 5, lines 39-50; col. 39, lines 10-13), each signal processing unit

being clocked by a common clock signal; a mode line connected to each signal processing unit

for switching each signal processing unit between a transmit mode and a receive mode; and a

control line to which each signal processing unit is connected, the control line communicating

flow control information either in the transmit mode to at least one of the preceding signal

processing units or in the receive mode to at least one of the following signal processing units

(col. 5, lines 39-50; In col. 39, lines 25-35; Meinecke et al. discloses four connections between

the HRSTs, 48 and 72. HSRT 48 has a receive data line, RXDATA, a receive clock line,

RXCLK, a transmit data line TXDATA and a transmit clock line TXCLK. The HSRT 48 signals

are connected to HSRT 72 signals, TXDATA, TXCLK, RXDATA and RXCLK, respectively, to

form a full duplex system. Thus the signal processing units (HSRTs) are connected in sequence

and to a common clock (TXCLK, RXCLK) and a mode line (RXDATA, TXDATA) or

equivalent for switching between transmit and receive modes. The TXDATA, RXDATA lines

would also constitute control lines communicating control flow information to at least one of the

preceding signal processing units and in the receive mode to at least one of the following signal

processing units. Meinecke et al. also discloses *inherent flow control* of the devices (col. 5, lines

39-50)).

     (2) With regard to claim 2, Meinecke et al. discloses communication device for

processing an outgoing packet, the device comprising: a plurality of signal processing units

connected in sequence (col. 5, lines 39-50; col. 39, lines 10-13), each signal processing unit

being clocked by a common clock signal; and a control line to which each signal processing unit

is connected, the control line communicating flow control information to stall at least one of the

preceding signal processing units for feedback control of the signal processing units (col. 5, lines

39-50; In col. 39, lines 25-35; Meinecke et al. discloses four connections between the HRSTs, 48

and 72. HSRT 48 has a receive data line, RXDATA, a receive clock line, RXCLK, a transmit

data line TXDATA and a transmit clock line TXCLK. The HSRT 48 signals are connected to

HSRT 72 signals, TXDATA, TXCLK, RXDATA and RXCLK, respectively, to form a full

duplex system. Thus the signal processing units (HSRTs) are connected to a common clock

(TXCLK, RXCLK) and a mode line (RXDATA, TXDATA) or equivalent for switching between

transmit and receive modes. The TXDATA, RXDATA lines would also constitute control lines

communicating control flow information to at least one of the preceding signal processing units

and in the receive mode to at least one of the following signal processing units. Meinecke et al.

also discloses *inherent flow control* of the devices (col. 5, lines 39-50; In col. 48, line 51-col. 50,

line 15, Meinecke et al. discloses flow control by the host adapter which comprises a HSRT to

prevent overflow of the output buffer in the data concentrator which also comprises a HSRT. The

receive buffer of the data concentrator is polled and flow control initiated in the preceding host

adapter (to halt input flow (stall)) accordingly for feedback control of the host adapter/ signal

processing unit).

(3) With regard to claim 3, Meinecke et al. discloses a communication device for

processing an incoming packet, the device comprising: a plurality of signal processing units

connected in sequence (col. 5, lines 39-50; col. 39, lines 10-13) thereby forming a signal

processing chain, each signal processing unit being clocked by a common clock signal; and a

control line to which each signal processing unit is connected, the control line communicating

flow control information to stall at least one of the signal processing units following in the signal

processing chain for feedforward control of the signal processing units (col. 5, lines 39-50; In

col. 39, lines 25-35; Meinecke et al. discloses four connections between the HRSTs, 48 and 72.

HSRT 48 has a receive data line, RXDATA, a receive clock line, RXCLK, a transmit data line

TXDATA and a transmit clock line TXCLK. The HSRT 48 signals are connected to HSRT 72

signals, TXDAT, TXCLK, RXDATA and RXCLK, respectively, to form a full duplex system.

Thus the signal processing units (HSRTs) are connected in sequence thereby forming a signal

processing chain and connected to common clock (TXCLK, RXCLK) and a mode line

(RXDATA, TXDAT) or equivalent for switching between transmit and receive modes. The

TXDATA, RXDATA lines would also constitute control lines communicating control flow

information to at least one of the preceding signal processing units and in the receive mode to at

least one of the following signal processing units. Meinecke et al. also discloses *inherent flow*

control of the devices (col. 5, lines 39-50; In col. 48, line 51-col. 50, line 15, Meinecke et al.

Meinecke et al. discloses flow control by the host adapter which comprises a HSRT to prevent

overflow of the output buffer in the data concentrator which also comprises a HSRT. The receive

buffer of the data concentrator is polled and flow control initiated in the preceding host adapter

(to halt input flow (stall)) accordingly for feedback control of the host adapter/ signal processing

unit). Since input flow into the data concentrator is halted, the control flow information would

inherently result in stall (receiving of data) in the data concentrator for feedforward control of the

signal processing unit).

　　　(4) With regard to claim 4, Meinecke et al. also discloses the device according to claim 1,

wherein each signal processing unit comprises a multiplexing function (col. 3, lines 44-51;

Meinecke et al. discloses the data concentrators (which comprise a HSRT) performing a

multiplexing function).

　　　(5) With regard to claim 5, Meinecke et al. also discloses the device according to claim 2,

wherein each signal processing unit comprises a multiplexing function (col. 3, lines 44-51;

Meinecke et al. discloses the data concentrators (which comprise a HSRT) performing a

multiplexing function).

　　　(6) With regard to claim 6, Meinecke et al. also discloses the device according to claim 3,

wherein each signal processing unit comprises a multiplexing function (col. 3, lines 44-51;

Meinecke et al. discloses the data concentrators (which comprise a HSRT) performing a

multiplexing function).

　　　(7) With regard to claim 7, Meinecke et al. also discloses the device according to claim 1,

wherein each signal processing unit comprises a multiplexer at its input and a demultiplexer at its

output (Fig. 2 discloses data concentrator receiving serial communications and parallel communications, inherently implying a multiplexer at its input and a demultiplexer at its output).

(8) With regard to claim 8, Meinecke et al. also discloses the device according to claim 2, wherein each signal processing unit comprises a multiplexer at its input and a demultiplexer at its output (Fig. 2 discloses data concentrator receiving serial communications and parallel communications, inherently implying a multiplexer at its input and a demultiplexer at its output).

(9) With regard to claim 9, Meinecke et al. also discloses the device according to claim 3, wherein each signal processing unit comprises a multiplexer at its input and a demultiplexer at its output (Fig. 2 discloses data concentrator receiving serial communications and parallel communications, inherently implying a multiplexer at its input and a demultiplexer at its output).

(10) Regarding claim 16, Meinecke et al. also discloses the device according to claim 1, wherein the flow control information comprises a hold information indicating to the signal processing units receiving the hold information to stop processing (col. 26, lines 35-40, col. 49, lines 42-46).

(11) Regarding claim 17, Meinecke et al. also discloses the device according to claim 2, wherein the flow control information comprises a hold information indicating to the signal processing units receiving the hold information to stop processing (col. 26, lines 35-40, col. 49, lines 42-46).

(12) Regarding claim 18, Meinecke et al. also discloses the device according to claim 3, wherein the flow control information comprises a hold information indicating to the signal processing units receiving the hold information to stop processing (col. 26, lines 35-40, col. 49, lines 42-46).

(13) Regarding claim 19, Meinecke et al. also discloses wherein each signal processing

unit is usable for the transmit and receive mode (col. 39, lines 25-35; Meinecke et al. discloses

the HSRTs connected to form a full duplex system).

(14) With regard to claim 20, Meinecke et al. discloses a transceiver unit (Fig. 2,

comprised of Host Adapter, 18, Data Concentrator, 28) adapted to communicate with a buffer

unit (col. 36, lines 14-19, I/O buffer of host CPU) via a bus system (20, system bus), the

transceiver comprising a transceiver controller (Host Adapter CPU, 40); and a communication

device (Fig. 2; Host Adapter, 18 and Data Concentrator, 28) both transceiver controller and

communication device being interconnected, said communication device including a plurality of

signal processing (HSRT) units connected in sequence (col. 5, lines 39-50; col. 39, lines 10-13),

each signal processing unit being clocked by a common clock signal; and a control line to which

each signal processing unit is connected, the control line communicating flow control

information to stall at least one of the preceding signal processing units for feedback control of

the signal processing units (col. 5, lines 39-50; In col. 39, lines 25-35; Meinecke et al. discloses

four connections between the HRSTs, 48 and 72. HSRT 48 has a receive data line, RXDATA, a

receive clock line, RXCLK, a transmit data line TXDATA and a transmit clock line TXCLK.

The HSRT 48 signals are connected to HSRT 72 signals, TXDATA, TXCLK, RXDATA and

RXCLK, respectively, to form a full duplex system. Thus the signal processing units (HSRTs)

are connected to a common clock (TXCLK, RXCLK) and a mode line (RXDATA, TXDATA) or

equivalent for switching between transmit and receive modes. The TXDATA, RXDATA lines

would also constitute control lines communicating control flow information to at least one of the

preceding signal processing units and in the receive mode to at least one of the following signal

processing units. Meinecke et al. also discloses *inherent flow control* of the devices (col. 5, lines

39-50; In col. 48, line 51-col. 50, line 15, Meinecke et al. discloses flow control by the host

adapter which comprises a HSRT to prevent overflow of the output buffer in the data

concentrator which also comprises a HSRT. The receive buffer of the data concentrator is polled

and flow control initiated in the preceding host adapter (to halt input flow (stall)) accordingly for

feedback control of the host adapter/ signal processing unit).

(15) With regard to claim 21, Meinecke et al. discloses a transceiver unit adapted to

communicate with a buffer unit via a bus system, the transceiver unit comprising a transceiver

controller (Fig. 2, Host Adapter CPU, 40); and a communication device (Fig. 2; Host Adapter, 18

and Data Concentrator, 28), both transceiver controller and communication device being

interconnected, said communication device comprising a plurality of signal processing units

connected in sequence (col. 5, lines 39-50; col. 39, lines 10-13), each signal processing unit

being clocked by a common clock signal; and a control line to which each signal processing unit

is connected, the control line communicating flow control information to stall at least one of the

preceding signal processing units for feedback control of the signal processing units (col. 5, lines

39-50; In col. 39, lines 25-35; Meinecke et al. discloses four connections between the HRSTs, 48

and 72. HSRT 48 has a receive data line, RXDATA, a receive clock line, RXCLK, a transmit

data line TXDATA and a transmit clock line TXCLK. The HSRT 48 signals are connected to

HSRT 72 signals, TXDATA, TXCLK, RXDATA and RXCLK, respectively, to form a full

duplex system. Thus the signal processing units (HSRTs) are connected to a common clock

(TXCLK, RXCLK) and a mode line (RXDATA, TXDATA) or equivalent for switching between

transmit and receive modes. The TXDATA, RXDATA lines would also constitute control lines

communicating control flow information to at least one of the preceding signal processing units

and in the receive mode to at least one of the following signal processing units. Meinecke et al.

also discloses *inherent flow control* of the devices (col. 5, lines 39-50; In col. 48, line 51-col. 50,

line 15, Meinecke et al. discloses flow control by the host adapter which comprises a HSRT to

prevent overflow of the output buffer in the data concentrator which also comprises a HSRT. The

receive buffer of the data concentrator is polled and flow control initiated in the preceding host

adapter (to halt input flow (stall)) accordingly for feedback control of the host adapter/ signal

processing unit).

(16) With regard to claim 22, Meinecke et al. discloses a transceiver unit adapted to

communicate with a buffer unit via a bus system, the transceiver unit comprising a transceiver

controller (Fig. 2, Host Adapter CPU, 40); and a communication device (Fig. 2; Host Adapter, 18

and Data Concentrator, 28), both transceiver controller and communication device being

interconnected, said communication device including a plurality of signal processing units

connected in sequence (col. 5, lines 39-50; col. 39, lines 10-13) thereby forming a signal

processing chain, each signal processing unit being clocked by a common clock signal; and a

control line to which each signal processing unit is connected, the control line communicating

flow control information to stall at least one of the signal processing units following in the signal

processing chain for feedforward control of the signal processing units (col. 5, lines 39-50; In

col. 39, lines 25-35; Meinecke et al. discloses four connections between the HRSTs, 48 and 72.

HSRT 48 has a receive data line, RXDATA, a receive clock line, RXCLK, a transmit data line

TXDATA and a transmit clock line TXCLK. The HSRT 48 signals are connected to HSRT 72

signals, TXDAT, TXCLK, RXDATA and RXCLK, respectively, to form a full duplex system.

Thus the signal processing units (HSRTs) are connected in sequence thereby forming a signal

processing chain and connected to common clock (TXCLK, RXCLK) and a mode line

(RXDATA, TXDAT) or equivalent for switching between transmit and receive modes. The

TXDATA, RXDATA lines would also constitute control lines communicating control flow

information to at least one of the preceding signal processing units and in the receive mode to at

least one of the following signal processing units. Meinecke et al. also discloses *inherent flow*

control of the devices (col. 5, lines 39-50; In col. 48, line 51-col. 50, line 15, Meinecke et al.

Meinecke et al. discloses flow control by the host adapter which comprises a HSRT to prevent

overflow of the output buffer in the data concentrator which also comprises a HSRT. The receive

buffer of the data concentrator is polled and flow control initiated in the preceding host adapter

(to halt input flow (stall)) accordingly for feedback control of the host adapter/ signal processing

unit). Since input flow into the data concentrator is halted, the control flow information would

inherently result in stall (receiving of data) in the data concentrator for feedforward control of the

signal processing unit).

(17) With regard to claim 28, Meinecke et al. discloses a baseband system comprising a

communication device including a plurality of signal processing (HSRT) units connected in

sequence (col. 5, lines 39-50; col. 39, lines 10-13), each signal processing unit being clocked by

a common clock signal; a mode line connected to each signal processing unit for switching each

signal processing unit between a transmit mode and a receive mode; and a control line to which

each signal processing unit is connected, the control line communicating flow control

information either in the transmit mode to at least one of the preceding signal processing units or

in the receive mode to at least one of the following signal processing units (col. 5, lines 39-50; In

col. 39, lines 25-35; Meinecke et al. discloses four connections between the HRSTs, 48 and 72.

HSRT 48 has a receive data line, RXDATA, a receive clock line, RXCLK, a transmit data line

TXDATA and a transmit clock line TXCLK. The HSRT 48 signals are connected to HSRT 72

signals, TXDATA, TXCLK, RXDATA and RXCLK, respectively, to form a full duplex system.

Thus the signal processing units (HSRTs) are connected in sequence and to a common clock

(TXCLK, RXCLK) and a mode line (RXDATA, TXDATA) or equivalent for switching between

transmit and receive modes. The TXDATA, RXDATA lines would also constitute control lines

communicating control flow information to at least one of the preceding signal processing units

and in the receive mode to at least one of the following signal processing units. Meinecke et al.

also discloses *inherent flow control* of the devices (col. 5, lines 39-50)).

Claim Rejections - 35 USC § 103

3.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

4.   Claims 10, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Meinecke

et al. (US Patent 5,319,754) as applied to claim 1, above, and further in view of Freiburg et al.

(US Patent 5,349,647).

As noted above, Meinecke et al. discloses all limitations of claim 1. Meinecke et al. does

not explictly teach wherein each signal processing unit is connected via a logic unit to the control line.

However, Freiburg et al. teaches in Fig(s). 3A, 3B, signal processing units (252-256) connected via a logic unit to a control line (col. 14, lines 12-22). It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Freiburg such that the direction of each signal processing unit and accordingly data flow can be alternately programmable.

Though Freiburg is silent as to the make up of the logic unit, one or ordinary skill in the art would readily recognize that the use intended by Freiburg could readily be implemented using an OR gate or any combination of logic and thus would be a mere design choice of the user.

5.   Claims 11, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Meinecke et al. (US Patent 5,319,754) as applied to claim 2, above, and further in view of Freiburg et al. (US Patent 5,349,647).

As noted above, Meinecke et al. discloses all limitations of claim 1. Meinecke et al. does not explictly teach wherein each signal processing unit is connected via a logic unit to the control line.

However, Freiburg et al. teaches in Fig(s). 3A, 3B, signal processing units (252-256) connected via a logic unit to a control line (col. 14, lines 12-22). It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Freiburg such that the direction of each signal processing unit and accordingly data flow can be alternately programmable.

Though Freiburg is silent as to the make up of the logic unit, one or ordinary skill in the art would readily recognize that the use intended by Freiburg could readily be implemented using an OR gate or any combination of logic and thus would be a mere design choice of the user.

6.   Claims 12, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Meinecke et al. (US Patent 5,319,754) as applied to claim 3, above, and further in view of Freiburg et al. (US Patent 5,349,647).

As noted above, Meinecke et al. discloses all limitations of claim 1. Meinecke et al. does not explictly teach wherein each signal processing unit is connected via a logic unit to the control line.

However, Freiburg et al. teaches in Fig(s). 3A, 3B, signal processing units (252-256) connected via a logic unit to a control line (col. 14, lines 12-22). It would have been obvious to one skilled in the art at the time of invention to incorporate the teachings of Freiburg such that the direction of each signal processing unit and accordingly data flow can be alternately programmable.

Though Freiburg is silent as to the make up of the logic unit, one or ordinary skill in the art would readily recognize that the use intended by Freiburg could readily be implemented using an OR gate or any combination of logic and thus would be a mere design choice of the user.

Conclusion

7.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a.) Dunning et al. discloses Method and Apparatus For Controlling The Flow of Data Between Servers Using Optimistic Transmitter in US 2003/0137939 A1.

b.) Optimal Parallel Processor Architecture For Real Time Multitasking in US Patent 5,590,323.

c.) Kuszmaul et al. discloses Parallel Computer System Including Arrangement For Quickly Draining Messages From Message Router in US Patent 5,390,298.

d.) Szczepanek discloses Signal Interface For Coupling A Network Front End Circuit To A Network Adapter Circuit in US Patent 5,299,193.

8.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence B Williams whose telephone number is 571-272-3037. The examiner can normally be reached on Monday-Friday (8:00-6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ghayour Mohammad can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Tesfaldet Bocure/
Primary Examiner, Art Unit 2611

lbw
May 12, 2009